USN | | | | | | | | | | |

10CS74

Seventh Semester B.E. Degree Examination, Dec.2015/Jan.2016
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the computer architecture. Explain the Bandwidth over Latency, and Benchmarks. **(06 Marks)**

b. Briefly explain the Amdahl's law. **(08 Marks)**

c. Assume a disk subsystem with the following components and MTTF:
   i) 10 disks, each rated at 1,000,000 hour MTTF
   ii) 1 SCSI controller, 5,00,000 – hour MTTF
   iii) 1 power supply, 2,00,000 – hour MTTF
   iv) 1 fan, 2,00,000 – hour MTTF
   v) 1SCSI cable, 1,000,000 – hour MTTF.
   Using the simplifying assumptions that the lifetimes are exponentially distributed and that failure are independent, compute the MTTF of the system as a whole. **(06 Marks)**

2 a. What is pipelining? List pipeline hazards. Explain any two in details. **(10 Marks)**

b. List and explain five different ways of classifying exception in a computer system. **(10 Marks)**

3 a. List the steps to unroll the code and schedule. **(04 Marks)**

b. What is the drawback of 1 – bit dynamic branch prediction method? Clearly state, how to overcome in 2 – bit prediction. Give the state transition diagram of 2 – bit predictor. **(06 Marks)**

c. With a neat diagram, give the basic structure of Tamasulo based MIPS FP unit and explain the various fields of reservation stations. **(10 Marks)**

4 a. Explain the basic VLIW approach List its drawbacks. **(10 Marks)**

b. With a neat diagram, explain the steps involved in handling an instruction, with a branch target buffer. **(10 Marks)**

PART – B

5 a. With a neat diagram, explain the basic structure of a centralized shared – memory and distributed memory multiprocessor. **(08 Marks)**

b. Define multiprocessor cache coherence. **(02 Marks)**

c. Explain the basic schemes of enforcing coherence in a shared memory multiprocessor system. **(10 Marks)**

6 a. Explain the six basic cache optimization techniques. **(12Marks)**

b. How to protect virtual memory and virtual machines? **(08 Marks)**

7 a. Assume we have a computer where the clock per instruction (CPI) is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? **(10 Marks)**

b. Explain in detail, the architecture support for protecting processes from each other via virtual memory. **(10 Marks)**

8 a. Explain in detail the hardware support for preserving exception behavior during speculation **(10 Marks)**

b. Write short notes on :
   i) The Itanium 2 processor **(05 Marks)**
   ii) IA – 64 register model **(05 Marks)**

* * * * *

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.